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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SCHMEISER, OLSEN + WATTS
3 LEAR JET LANE
SUITE 201
LATHAM, NY 12110

EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/683,872	IADANZA, JOSEPH A.
	Examiner	Art Unit
	Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,7,11,12,15,16 and 23-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-28* is/are allowed.

6)☒ Claim(s) *1, 3, 4, 6, 7, 11, 12, 15, 16, 29-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 6, 7, 11, 12, 15, 16, 30, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, as disclosed on figures 1-2 and their description in the instant application in view of Bohr (U.S. Patent No. 6,617,681). With regard to Claim 1, Applicant's admitted prior art discloses (see figure 1) a predefined block of functional circuitry (160) having a plurality of I/O pins (175).

Applicant's admitted prior art fails to disclose a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit. However, Bohr discloses (figure 15) a backside I/O pad (224) electrically connected to a backside via (ILD via) of an integrated circuit structure, since the interposer which contains said pad and via is taught by Bohr to include circuit functionality (column 6, lines 63-64) and more specifically I/O buffer circuits (column 7, lines 2-10). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die, through the use of the backside via, to a substrate (column 12, lines 35-37).

With regard to Claim 3, a further difference between the claimed invention and Applicant's admitted prior art is the claimed I/O pins formed in a lowest interconnect level of an integrated circuit chip, however it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include place the I/O pins in a desired interconnect level, for the purpose of optimizing circuit layout.

With regard to Claim 4, a further difference between the claimed invention and Applicant's admitted prior art is the claimed backside via formed in a bulk silicon substrate of the integrated circuit. However, Bohr discloses (figure 15) a backside I/O pad (224) electrically connected to a backside via (ILD via) of an integrated circuit structure, since the interposer which contains said pad and via is taught by Bohr to include circuit functionality (column 6, lines 63-64) and wherein the interposer is made of silicon (column 3, lines 64-65). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside via formed in a bulk silicon substrate of the integrated circuit, as suggested by Bohr, in order to allow the integration of passive or active circuit elements which can augment those that used in an integrated circuit (column 4, lines 21-24).

With regard to Claim 6, Applicant's admitted prior art discloses a predefined block of functional circuitry (160) that includes a first portion containing functional circuitry (165) and second portion (170) containing I/O pins (175), Applicant's admitted prior art fails to disclose a backside via connected to the second portion. However, Bohr discloses (figure 15) a backside I/O pad (224) electrically connected to a backside via (ILD via) of an integrated circuit structure,

since the interposer which contains said pad and via is taught by Bohr to include circuit functionality (column 6, lines 63-64) and more specifically I/O buffer circuits (column 7, lines 2-10). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die, through the use of the backside via, to a substrate (column 12, lines 35-37).

With regard to Claim 7, Applicant's admitted prior art discloses a plurality of front-side I/O pads (150) and additional I/O pins which are those not contained in I/O portion (170), each additional I/O pin electrically connected to one front-side I/O pad of the integrated circuit by a global wiring connection (see figure 1).

With regard to Claim 11, Applicant's admitted prior art discloses providing a predefined block of functional circuitry (160) having a plurality of I/O pins (175). Applicant's admitted prior art fails to disclose a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit. However, Bohr discloses (figure 15) a backside I/O pad (224) electrically connected to a backside via (ILD via) of an integrated circuit structure, since the interposer which contains said pad and via is taught by Bohr to include circuit functionality (column 6, lines 63-64) and more specifically I/O buffer circuits (column 7, lines 2-10). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside I/O pad electrically connected to each I/O pin through

a backside via of the integrated circuit, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die, through the use of the backside via, to a substrate (column 12, lines 35-37).

With regard to Claim 12, Applicant's admitted prior art discloses providing additional I/O pins which are those not contained in I/O portion (170) and electrically connecting each additional I/O pin to one front-side I/O pads (150) of the integrated circuit by a global wiring connection (see figure 1).

With regard to Claim 15, Applicant's admitted prior art discloses providing additional predefined I/O pins which are those not contained in I/O portion (170) and electrically connecting each additional I/O pin to one front-side I/O pads (150) of the integrated circuit by a global wiring connection (see figure 1).

With regard to Claim 16, a further difference between the claimed invention and Applicant's admitted prior art is the claimed backside via formed in a bulk silicon substrate of the integrated circuit. However, Bohr discloses (figure 15) a backside I/O pad (224) electrically connected to a backside via (ILD via) of an integrated circuit structure, since the interposer which contains said pad and via is taught by Bohr to include circuit functionality (column 6, lines 63-64) and wherein the interposer is made of silicon (column 3, lines 64-65). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside via formed in a bulk silicon substrate of the integrated circuit, as

suggested by Bohr, in order to allow the integration of passive or active circuit elements which can augment those that are used in an integrated circuit (column 4, lines 21-24).

With regard to Claims 30 and 33, a further difference between the claimed invention and Applicant's admitted prior art is the claimed backside I/O pad. However, Bohr discloses (figures 15 and 16) a first portion of the backside I/O pad (224), which is the portion closest to the via surface, that is in direct mechanical contact with the backside via, a second portion of the backside I/O pad, which is the outer portion farthest to the backside via that is not in direct contact with the backside via and wherein the second portion of the backside I/O pad is in direct mechanical contact, through contact (226) with a backside surface of the integrated circuit contained in the interposer.

With regard to Claim 35, a further difference between the claimed invention and Applicant's admitted prior art is the claimed I/O pins formed in a lowest interconnect level of an integrated circuit chip, however it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include place the I/O pins in a desired interconnect level, for the purpose of optimizing circuit layout.

Claims 29, 31, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, as disclosed on figures 1-2 and their description in the instant application in view of Bohr (U.S. Patent No. 6,617,681) and further in view of Ayon (U.S. Patent No. 6,399,516). With regard to Claims 29 and 32, Applicant's admitted prior art and Bohr

essentially disclose the claimed invention but fail to show, the claimed backside via comprising a slope sidewall. However, Ayon discloses (figure 1E) a semiconductor structure including a substrate (12) and a backside via (26) formed on the substrate, wherein the backside via has a sloped sidewall. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside via comprising a slope sidewall, as suggested by Ayon, in order to limit the amount of silicon to be etched on the upper part of the substrate when forming the backside via and thus allow remaining silicon material to be used for integration of circuit elements.

With regard to Claims 31 and 34, a further difference between the claimed invention and Applicant's admitted prior art and Bohr is, the claimed backside via extending through a buried oxide layer. However, Ayon discloses (figure 1E) a semiconductor structure including a substrate (12), a buried insulating layer (14) and a backside via (26) formed on the substrate and through the buried insulating layer. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to include the claimed backside via extending through a buried oxide layer, as suggested by Ayon, in order to enable electrical isolation of silicon elements, while providing the ability of making a backside electrical contact to the silicon layer (column 3, lines 27-33).

Allowable Subject Matter

3. Claims 23-28 are allowed, as stated in the previous office action.

Response to Arguments

4. Applicant's arguments filed have been fully considered but are not persuasive. Applicant first argues, "*Bohr does not disclose an integrated circuit comprising a backside I/O pad; i.e., the backside via in FIG. 15 is not disclosed by Bohr as being comprised by an integrated circuit*". However, the examiner notes that as stated in the rejection, Bohr discloses (figure 15) a backside I/O pad (224) electrically connected to a backside via (ILD via) of an integrated circuit structure, since the structure which contains said pad and via is taught by Bohr to include circuit functionality (column 6, lines 63-64) and more specifically I/O buffer circuits (column 7, lines 2-10). Further, Applicant does not specifically define the "integrated circuit" to be an integrated circuit die, thus any electrical structure that contains passive or active devices can be reasonably interpreted as comprising an integrated circuit. Therefore the claimed invention does not patentably or structurally distinguish form the cited references.

Applicant also argues regarding that "*the Examiner's argument for modifying Applicant's admitted prior art with the alleged teaching of Bohr is not persuasive.*" However, the examiner disagrees and notes that one with ordinary skill in the art, at the time of the invention, would be motivated to include the claimed backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit in the Applicant's admitted prior art structure, as suggested by Bohr, in order to electrically and mechanically couple an integrated circuit die, such as the die 100 of Applicant's admitted prior art, through the use of the backside via, to a substrate. Such coupling would result in additional external connections, which connections provide a good thermal expansion match and tight-pitch (column 12, lines 34-39).

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
3/17/05

GEORGE ECKERT
PRIMARY EXAMINER